

MODEL NAME : ZAVA1/ZAVC1
PCB NO : DA80011D000 LA-B015P-R1.0

Compal Confidential

Schematic Document

www.aitech1.ru

Intel BoardWell ULT

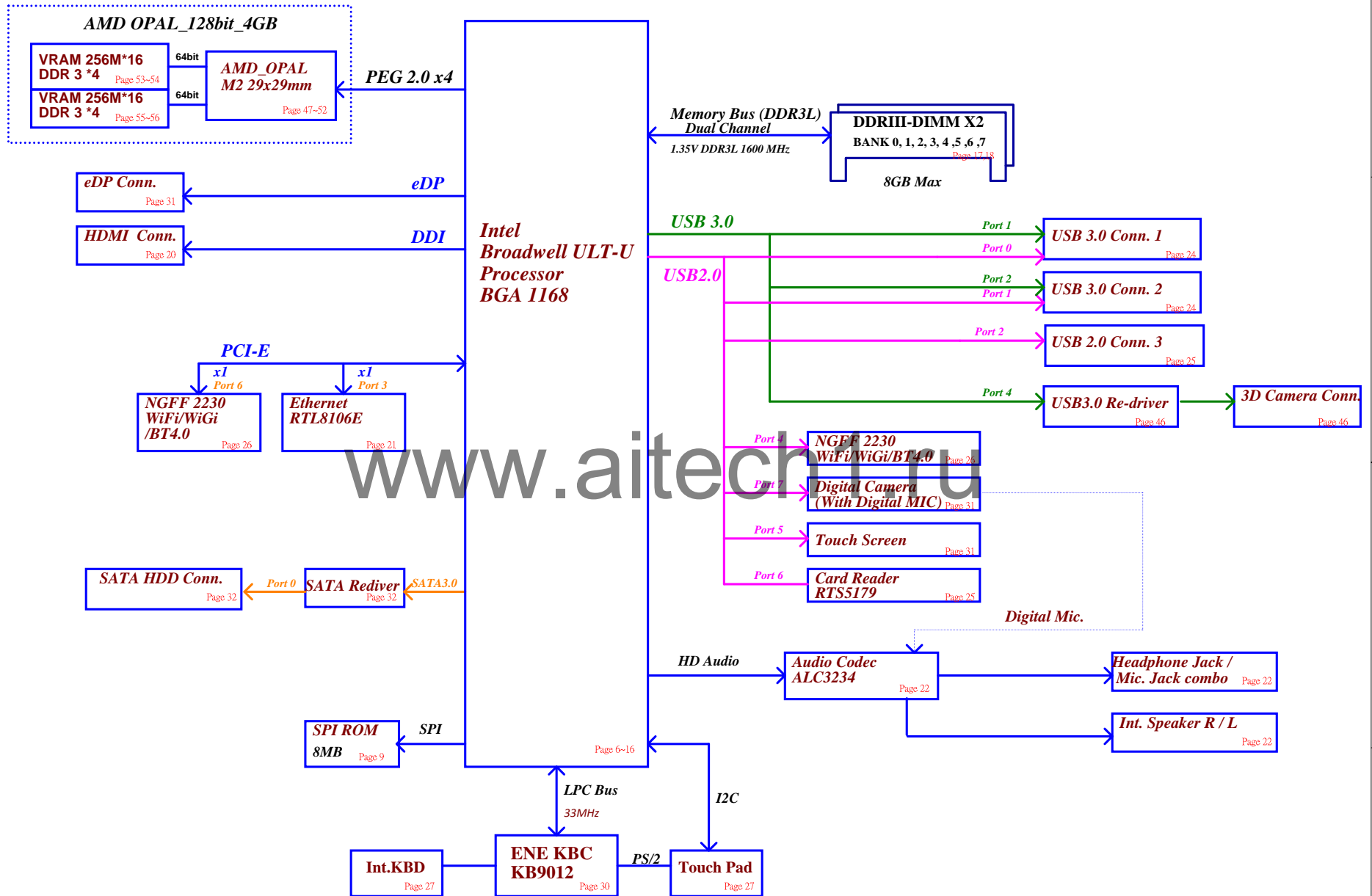
ZAVA1/ZAVC1

DIS AMD 25W/M2+DDR3x8

2014-10-17

Rev: 1.0

Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Document Number	
2014/10/17		2018/04/30		LA-B015P	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date: Friday, October 17, 2014	
				Sheet 1 of 56	
				Rev 1.0	



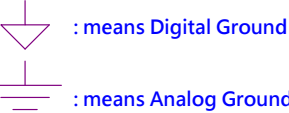
Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	VGA	DIMM	XD	Thermal Sensor	FFS
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012			V				
SMBCLK SMBDATA	ULT				V			V
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

Symbol Note :



HSW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)	DIS(OPAL)
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

BDW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)	DIS(OPAL)
0	1.0_3D CAM			
1		1.0_3D CAM		
2			1.0_3D CAM	
3	SSI(BDW)			
4		SSI(BDW)		
5			SSI(BDW)	
6	PT(BDW) SSI 3D CAM			
7		PT(BDW) SSI 3D CAM		
8			PT(BDW) SSI 3D CAM	
9	ST(BDW) PT 3D CAM			
10		ST(BDW) PT 3D CAM		
11			ST(BDW) PT 3D CAM	
12	1.0(BDW) ST 3D CAM			
13		1.0(BDW) ST 3D CAM		
14			1.0(BDW) ST 3D CAM	
15				SSI
16				PT
17				ST
18				1.0

CLOCK SIGNAL (Diff. 100MHz)

CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

USB3.0

Port1	USB connector 1
Port2	USB connector 2
Port3	
Port4	3D Camera

USB2.0

Port0	USB connector 1
Port1	USB connector 2
Port2	USB connector 3 (D/B)
Port3	
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera

PCI EXPRESS

Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (AMD JET/TOBAZ)
Lane 6	

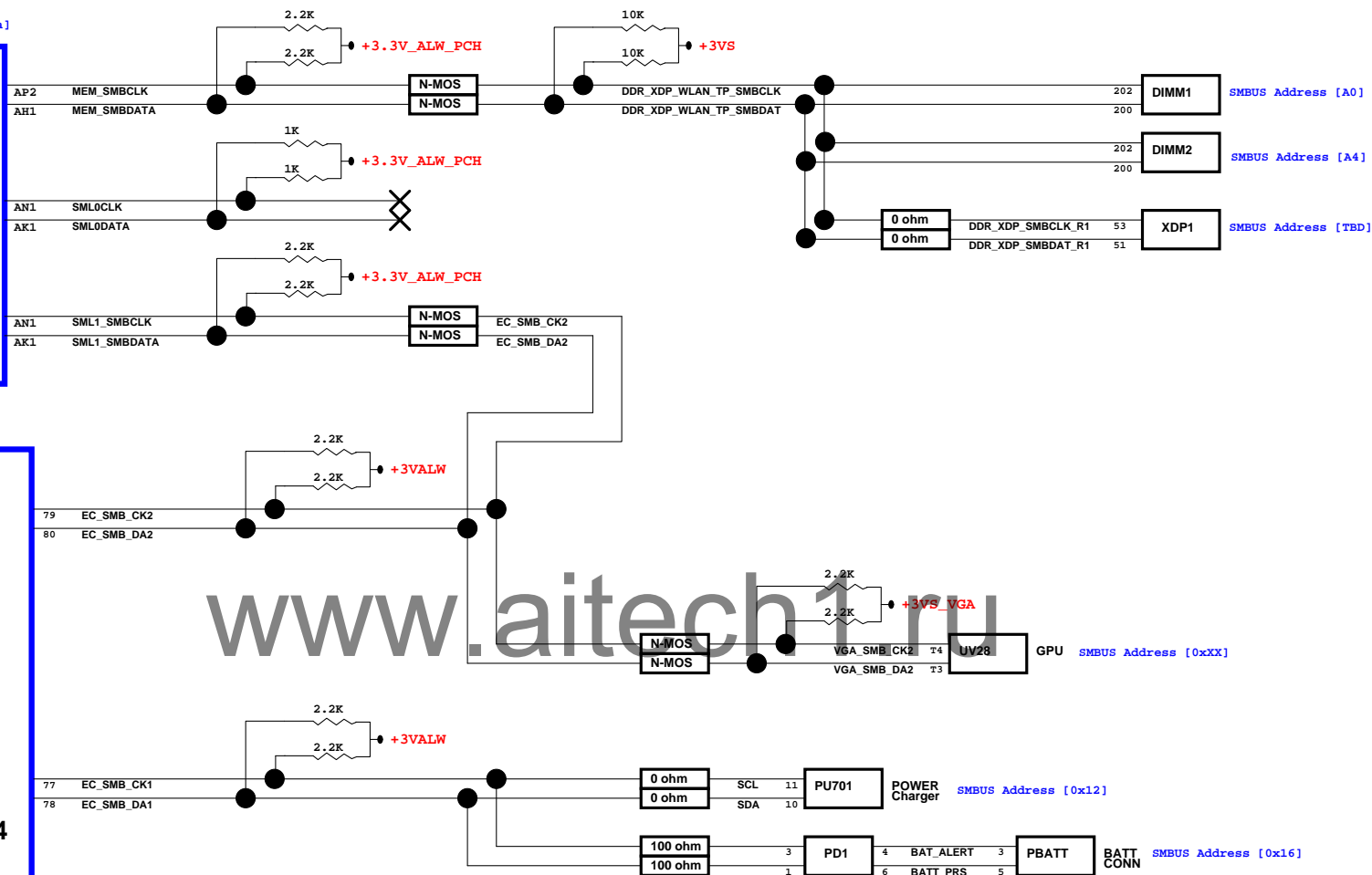
SATA

SATA0	HDD
SATA1	
SATA2	
SATA3	

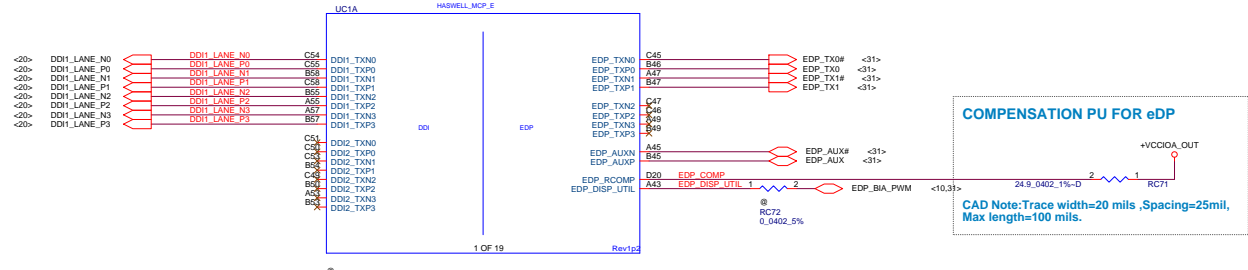
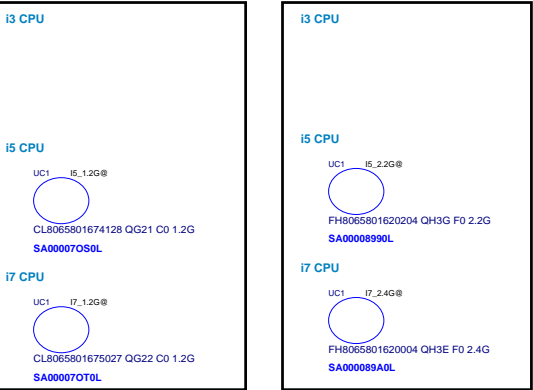
SMBUS Address [0x9a]

MCH
Shark bay

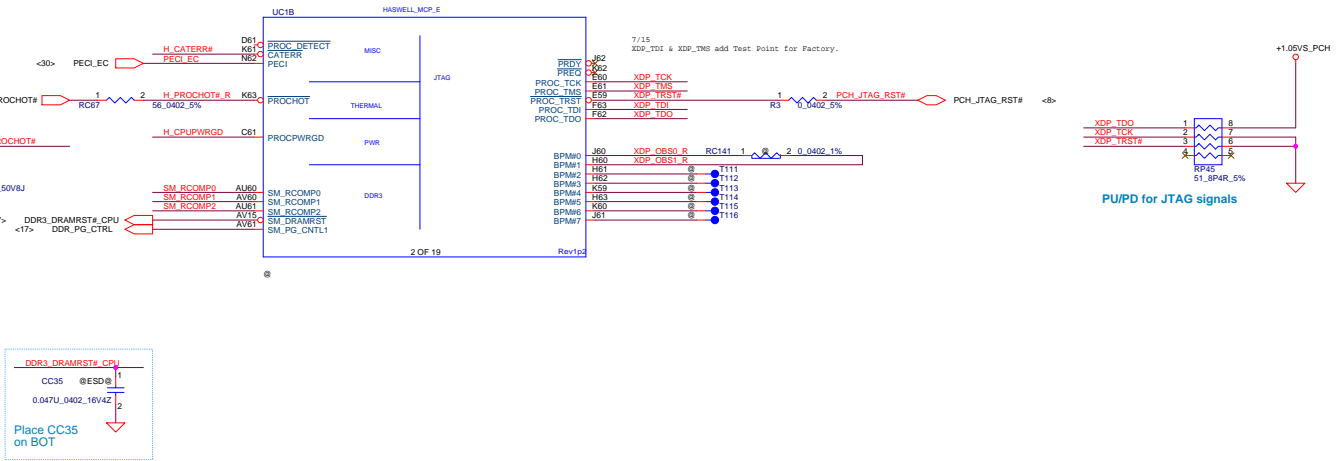
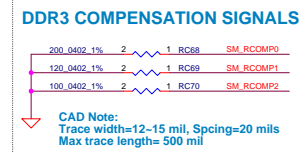
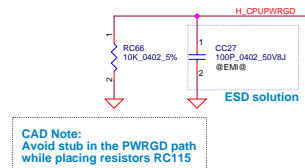
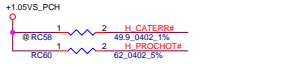
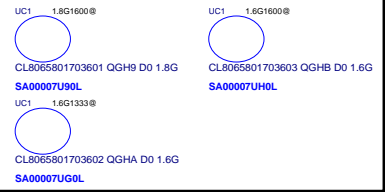
KBC
KB9012A4



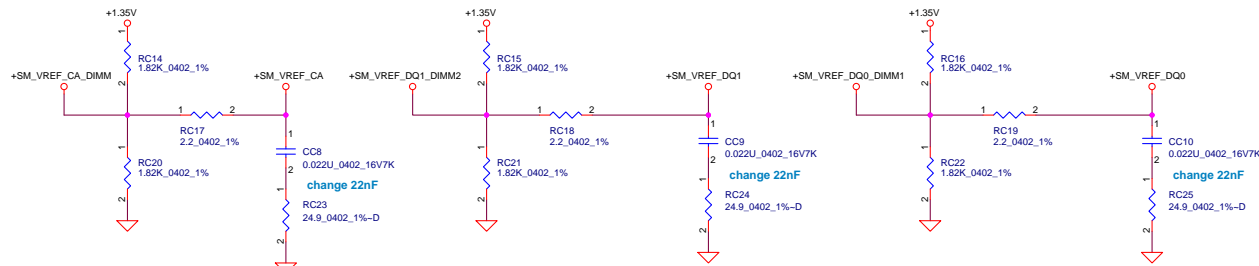
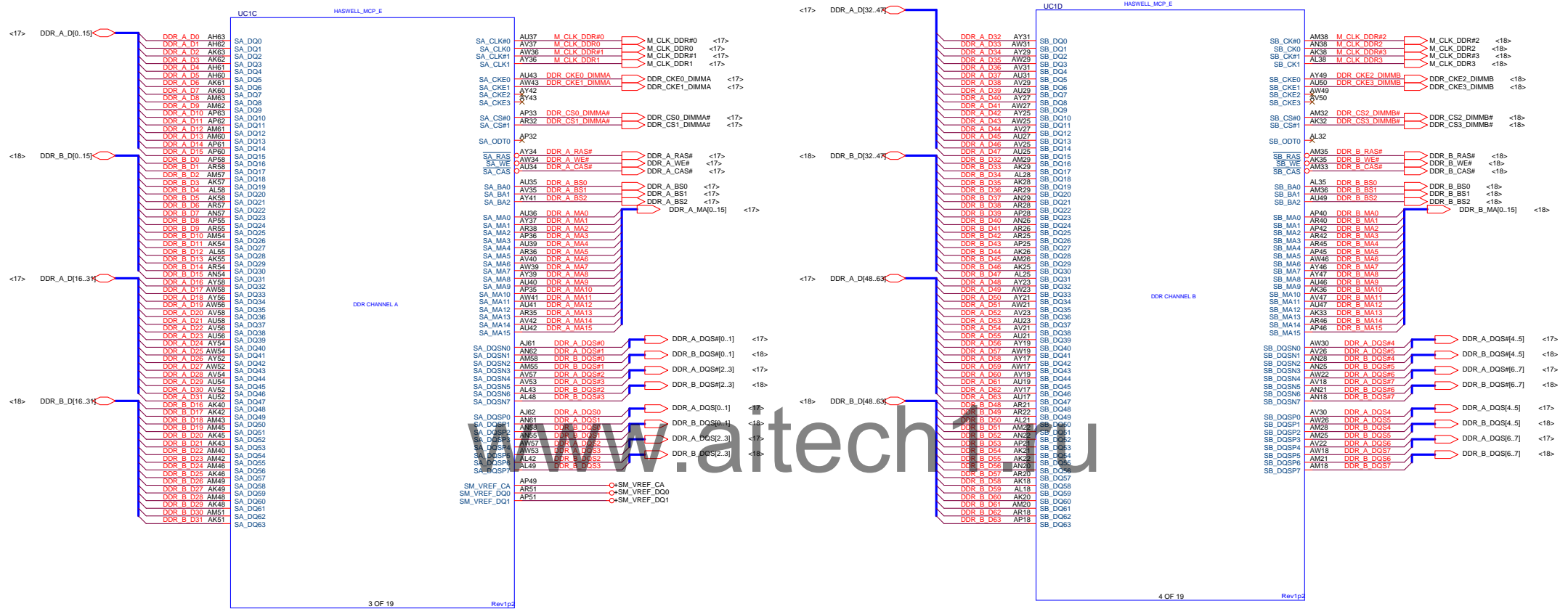
BDW_Pre-QS for DVT2 BDW_QS for DVT2



BDW (ES2) CPU for 3D / 4G

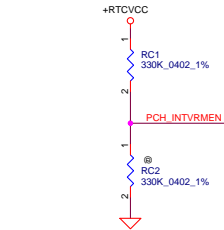


Interleaved Memory



confirm by intel request PDG P141

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title	MCP(3,4/19) DDR3
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT PRIOR WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-B015P
				Date	Wednesday, September 10, 2014
				Sheet	7 of 56

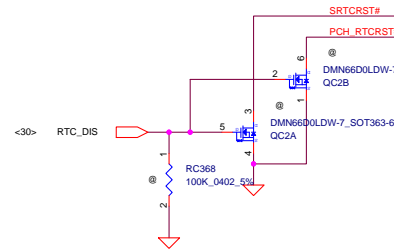


3VS

1 2 PCH_AZ_SDOUT

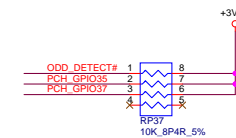
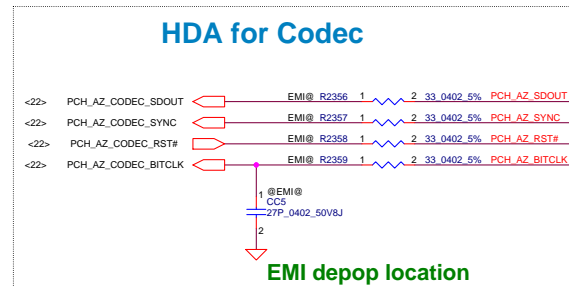
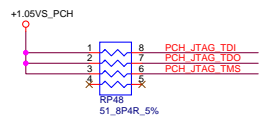
@RC3 1K_0402_5%

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED

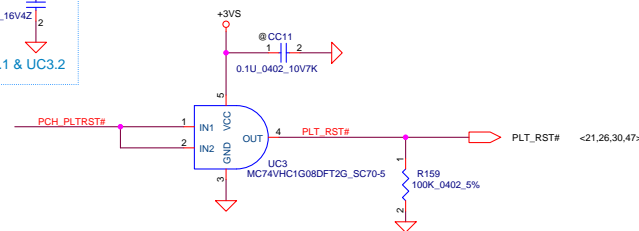
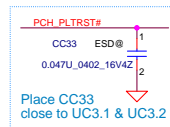
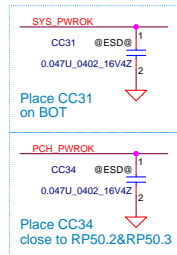


CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

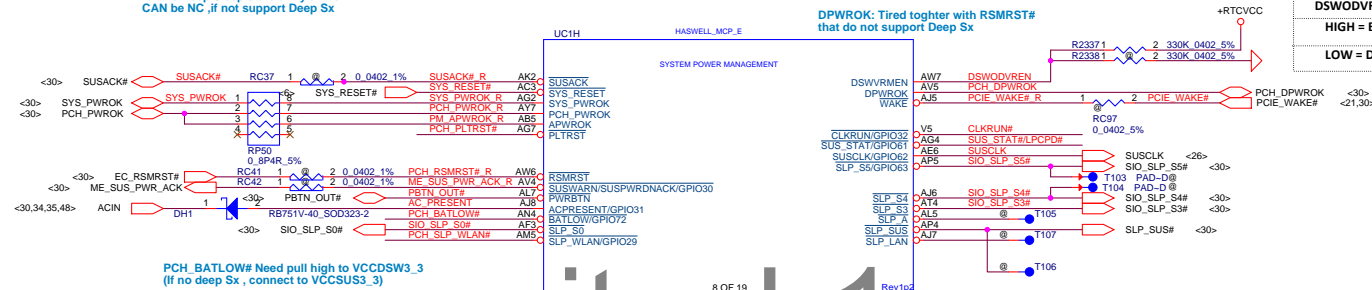


CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.
reference FFRD sch 0.5



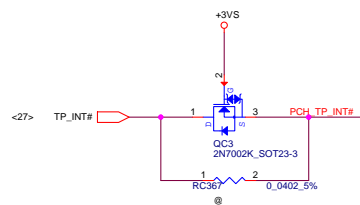
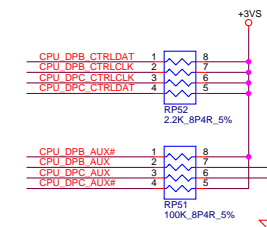
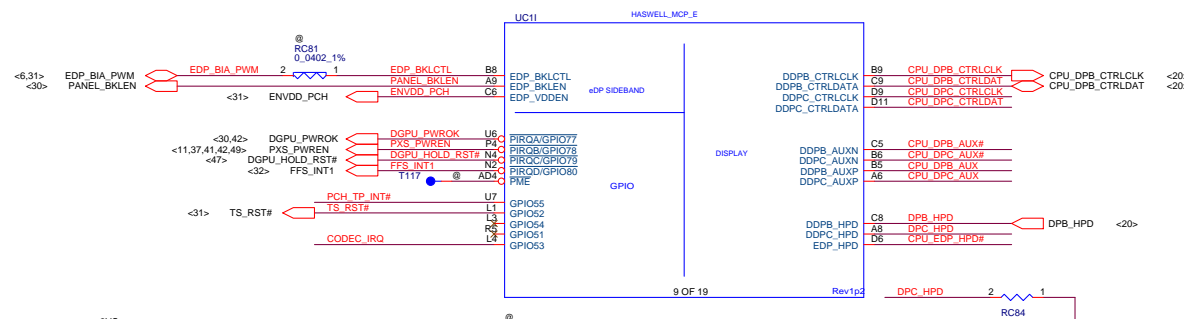
DSWODVREN - On Die DSW VR Enable
 * H : Enable(DEFAULT)
 L : Disable

DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

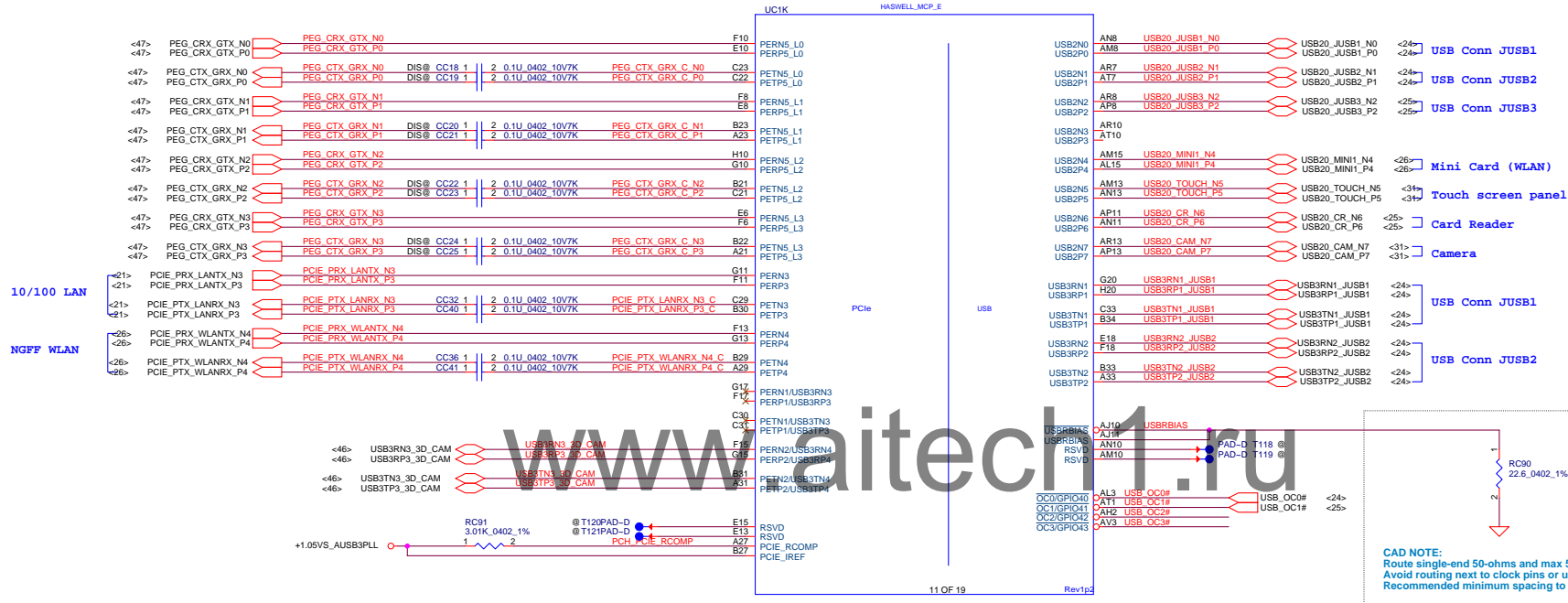


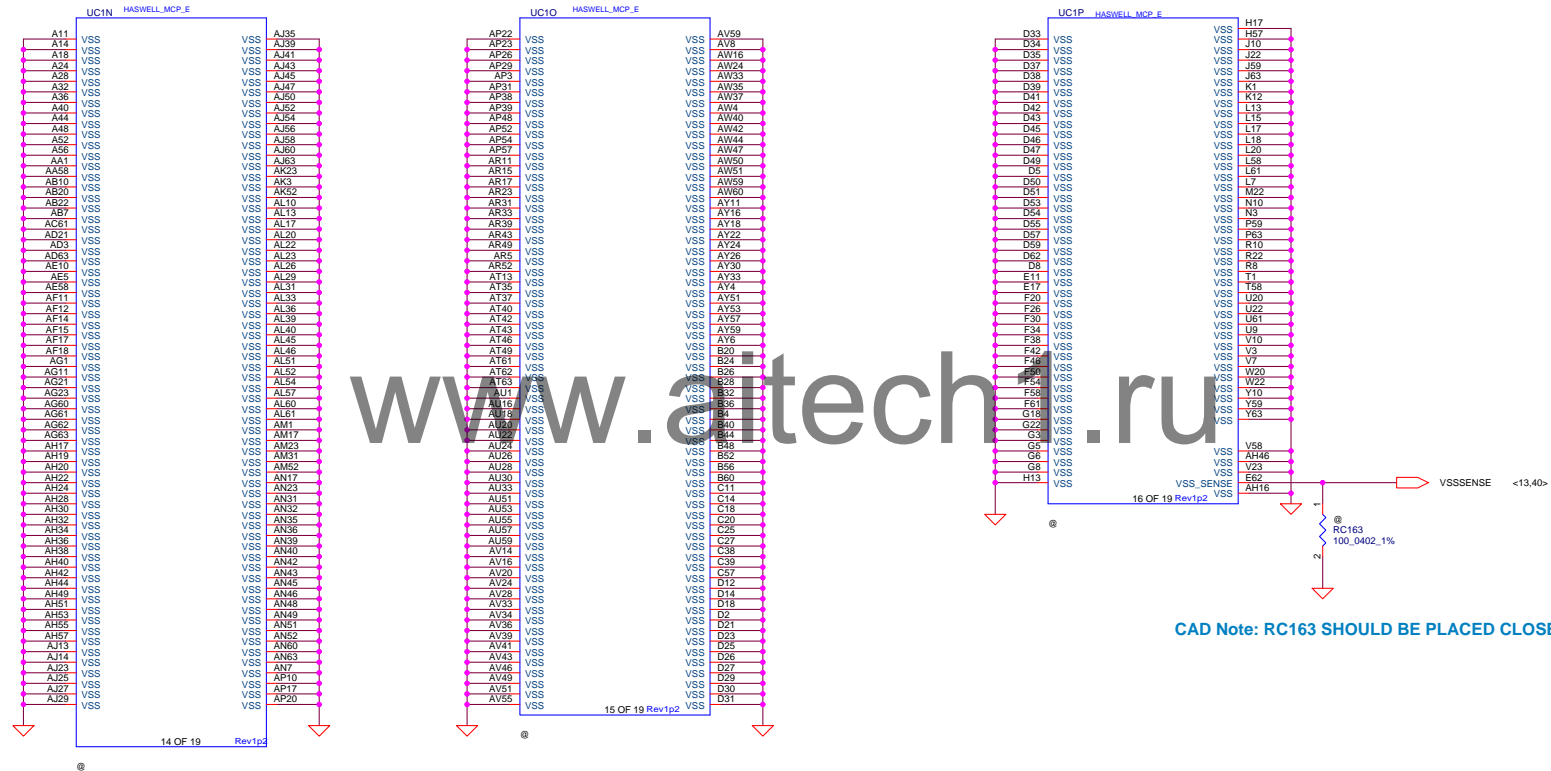
PCH_BATLOW# Need pull high to VCCDSW3_3
(If no deep Sx , connect to VCCSUS3_3)

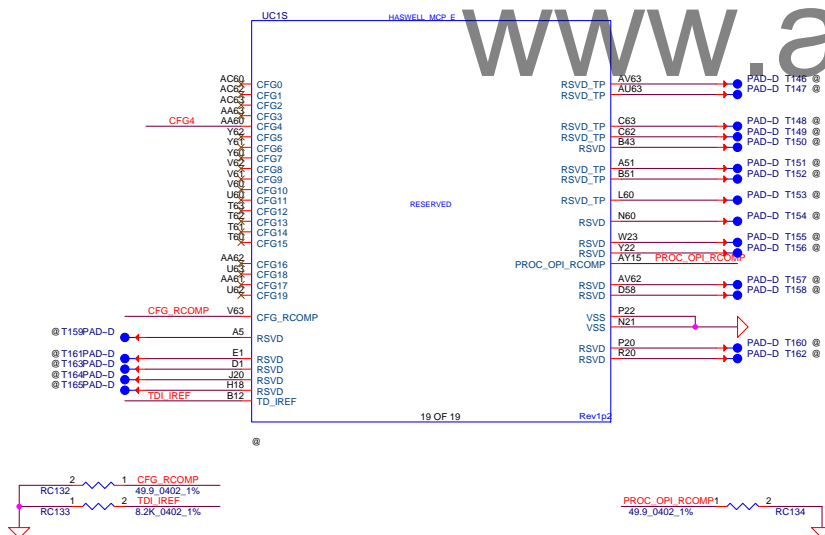
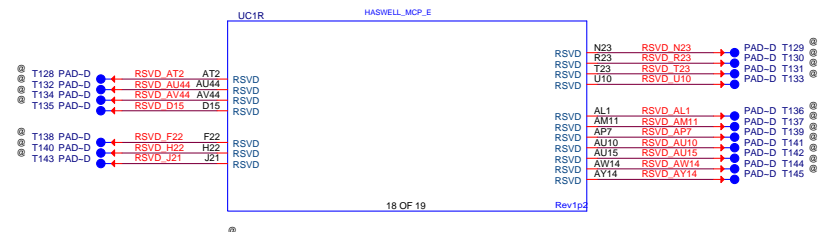
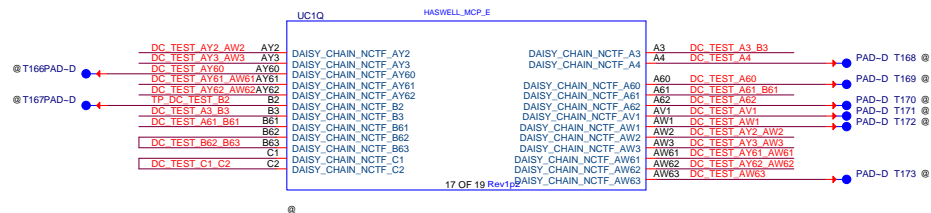
PCH_BATLOW# Need pull high to VCCDSW3_3
(If no deep Sx, connect to VCCSUS3_3)



Security Classification		Compal Secret Data		Compal Electronics, Inc. MCP(8,9/19) DDLEDP,GPIO	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.1
				LA-B015P Date: Wednesday, September 10, 2014	1 Sheet 10 of 56

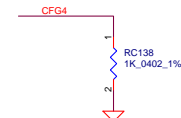




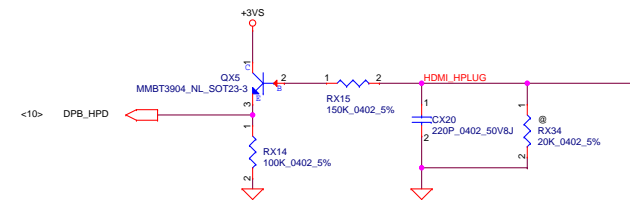
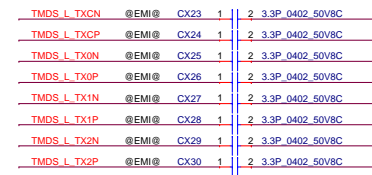
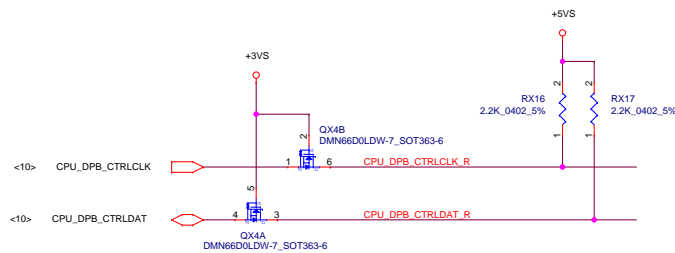
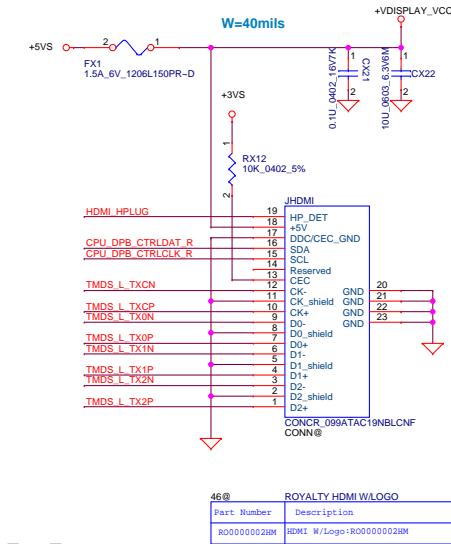
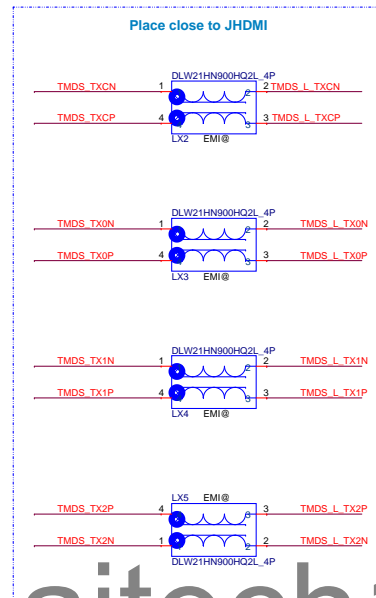
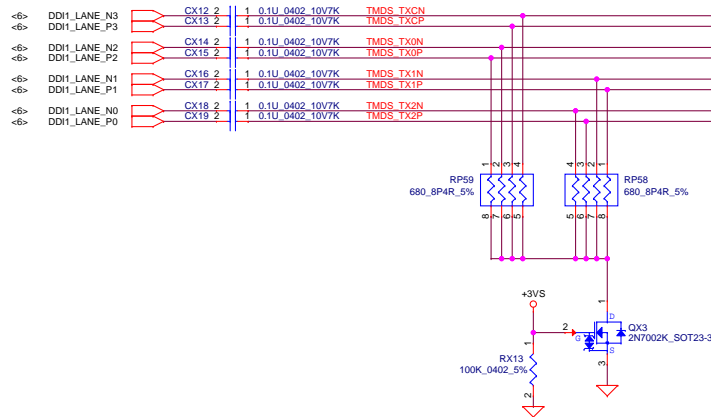


www.aitech1.ru

CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



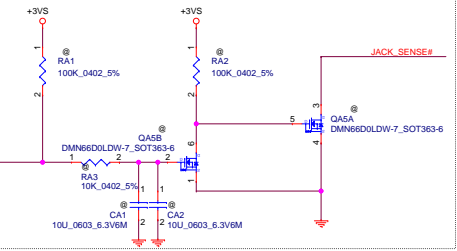
CA71, CA51 place close to Pin 26

CA53, CA55 change Value from 100U_0603_6.3V6M to 4.7U_0603_6.3V6K

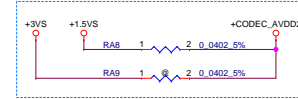
CA57, CA58 close to UA1 pin1

CA59 CA60 close to UA1 pin9

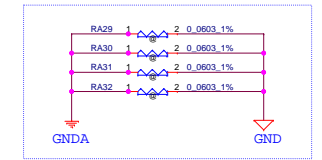
JACK_PLUG Delay circuitis



Reserve for HDA issue



Reserve for cancel Delay circuitis

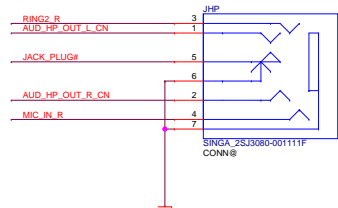


Place on the moat between GND & GNDA.

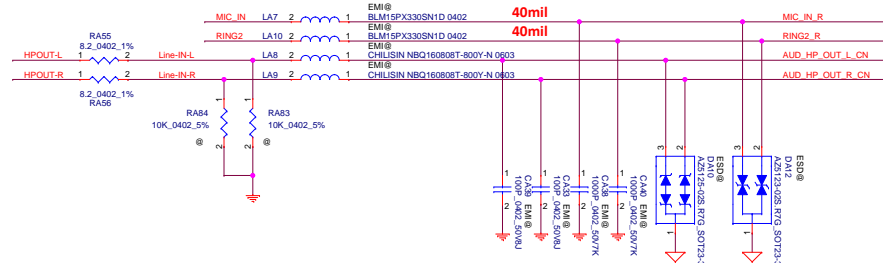
Close to UA1 Pin11,13,14,16

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R- Speaker 4 ohm : 40mil Speaker 8 ohm : 20mil

close to Codec



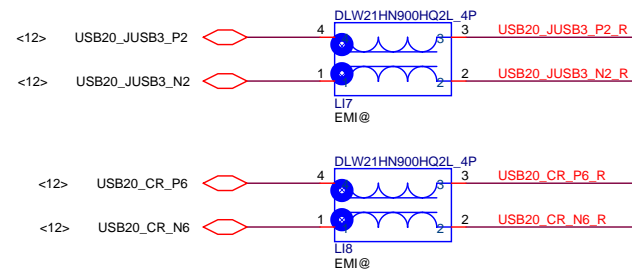
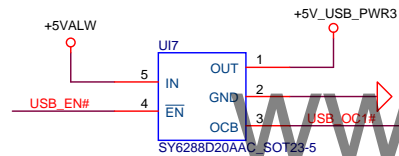
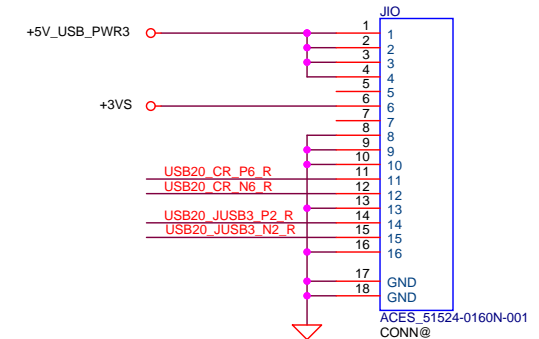
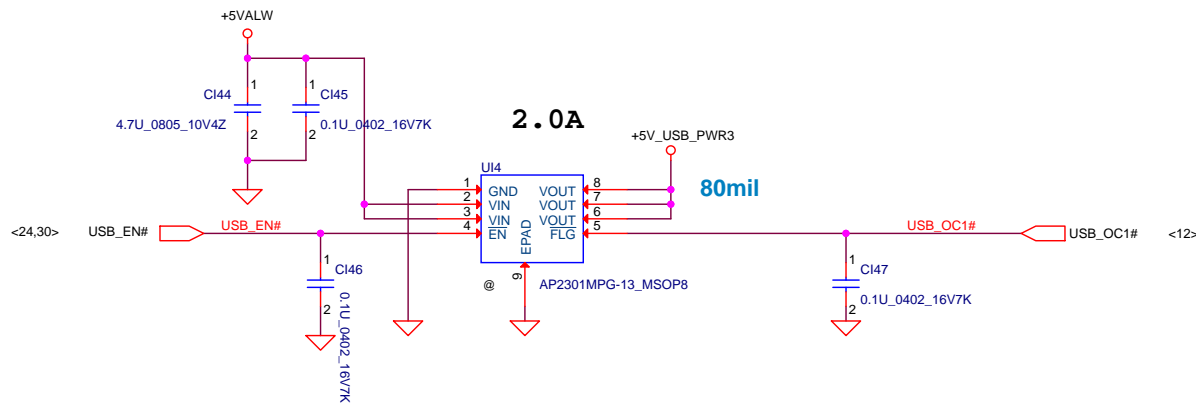
iPhone and Nokia type Combo Jack



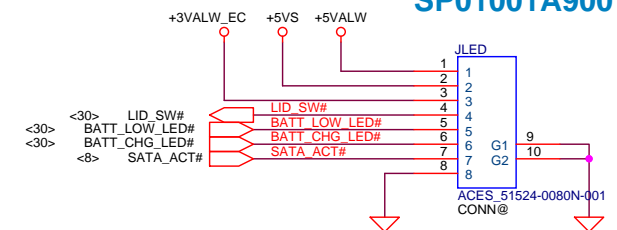
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPLET DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
				LA-B015P
				Rev 0.1
				Date: Friday, October 17, 2014
				Sheet 22 of 56

www.aitech1.ru

IO to MB CONN Substitute:SP01001FS00

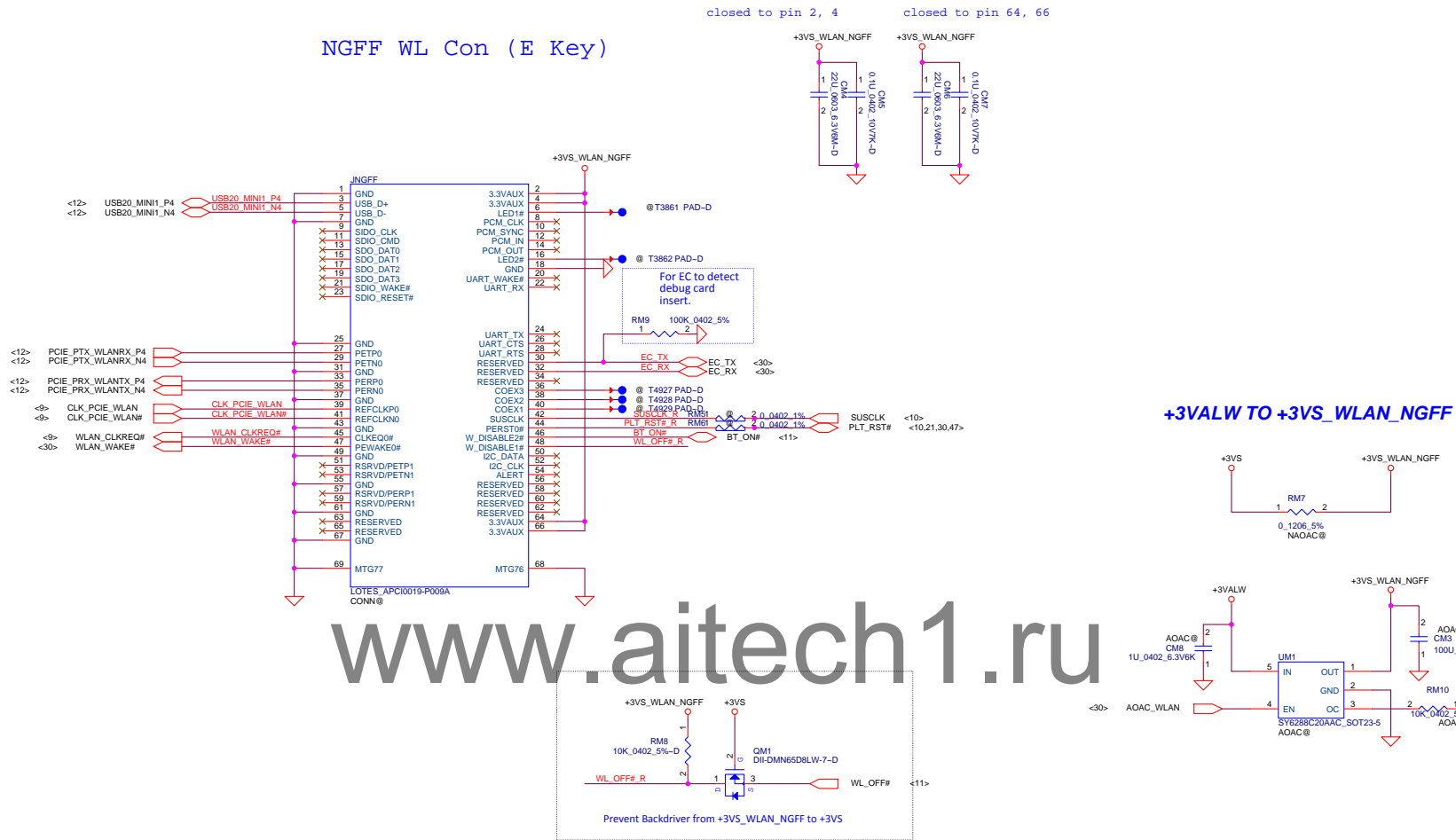


LED/B TO M/B SP01001A900



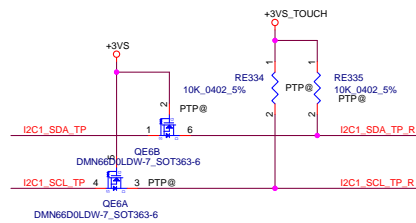
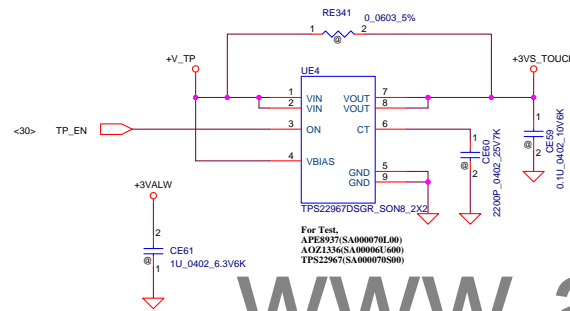
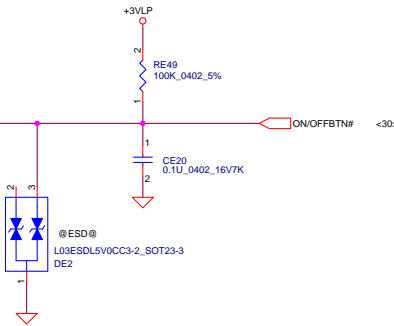
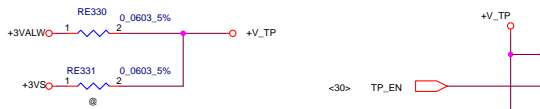
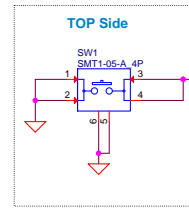
Security Classification				Compal Secret Data				Title	
Issued Date				2014/04/01		Deciphered Date		2015/04/30	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number		Rev		0.1	
Date:				Tuesday, September 16, 2014		Sheet		25 of 56	

NGFF WL Con (E Key)

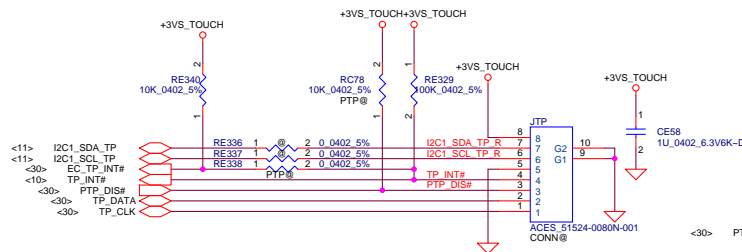


Power ON Circuit

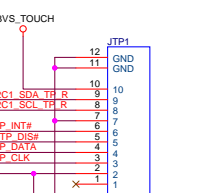
ON/OFF switch



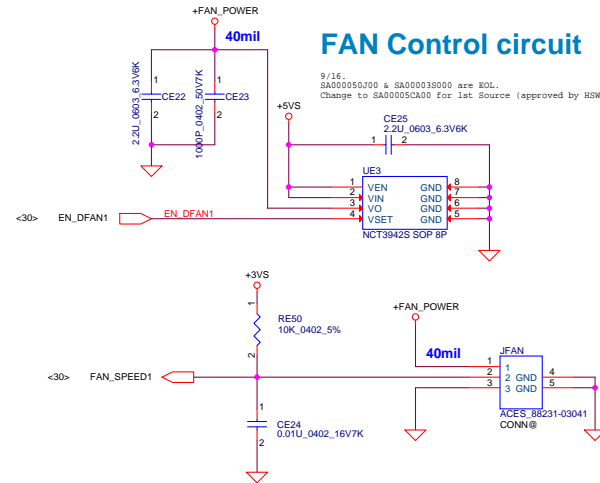
Touch pad



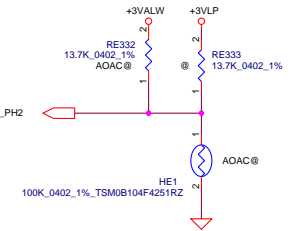
PTP



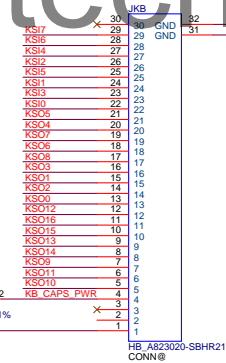
FAN Control circuit



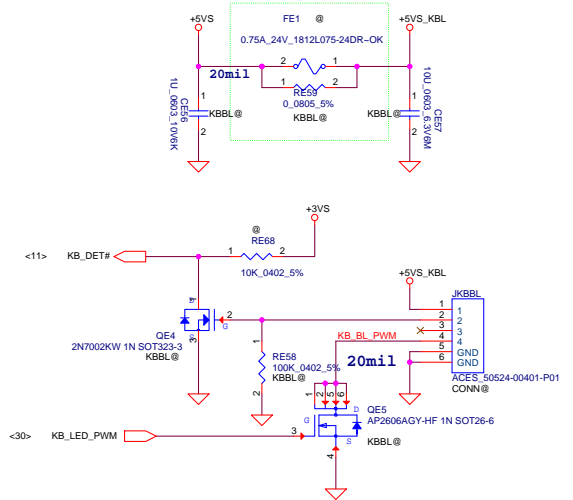
HE1 place around FAN area.



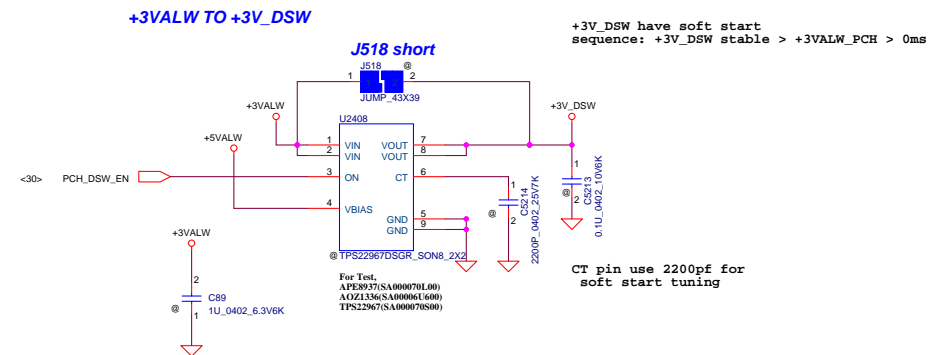
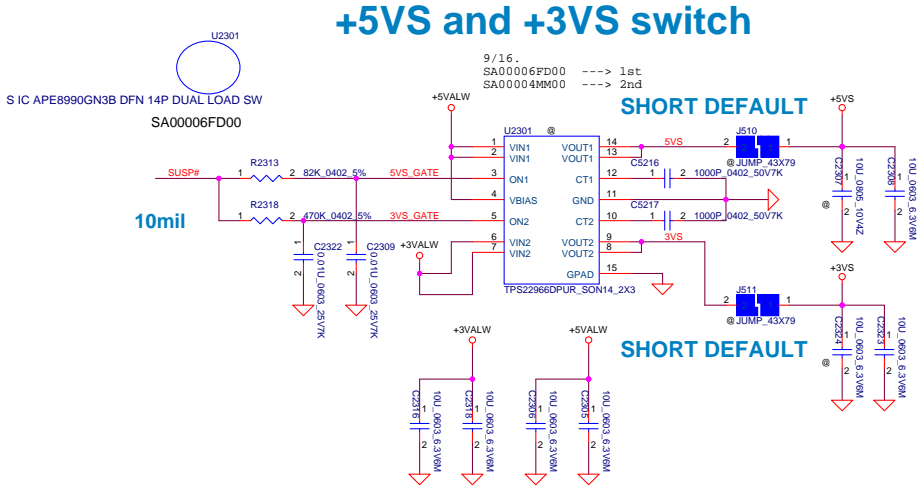
INT_KBD Connector



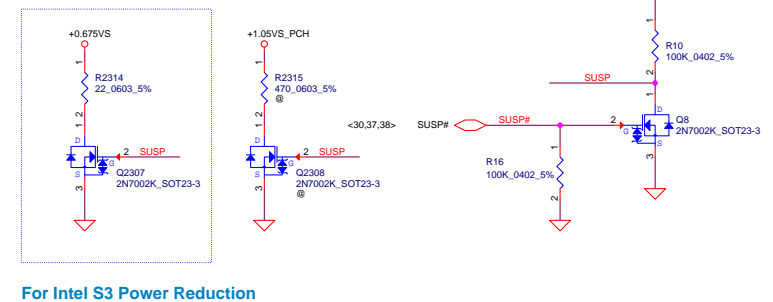
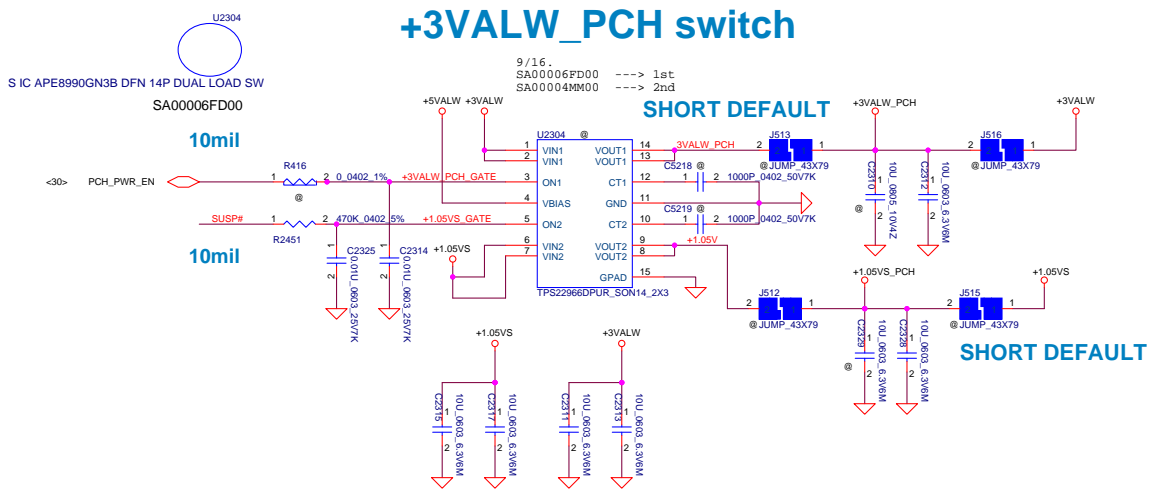
* Key Board Back Light



Security Classification		Compal Secret Data		Title	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	FAN / TP / PWR SW / KBBL	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF H&M DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-B015P	0.1
				Date	Friday, October 17, 2014
				Sheet	27 of 56



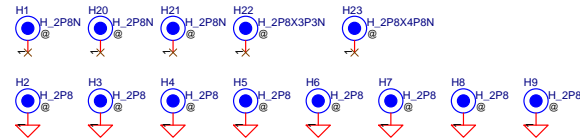
www.aitech1.ru



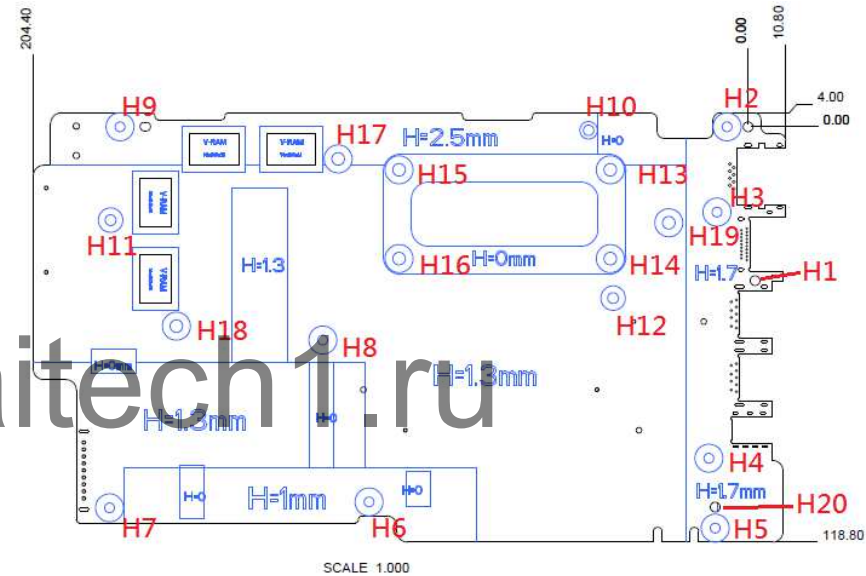
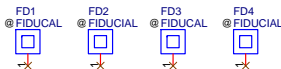
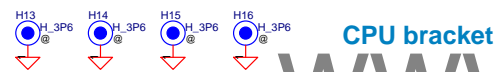
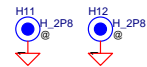
Security Classification		Compal Secret Data		Title	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	DC/DC Interface	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-B015P	0.1
Date: Tuesday, September 16, 2014				Sheet	28 of 56

Screw Hole

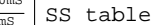
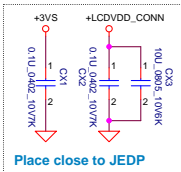
ZZZ
PCB 13G LA-B015P REV0 M/B
DA80011D000

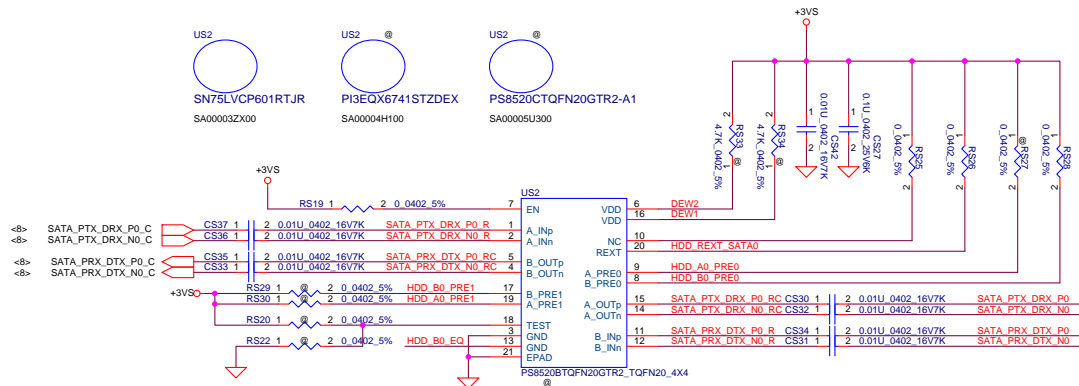


H10 Delete.
Layout informed PCB vendor to do PTH solution.
(Function is same as beofre.)

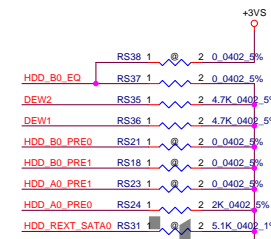


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title	Screw Hole
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-B015P
				Date	Wednesday, September 10, 2014
				Sheet	29 of 56
				Rev	0.1

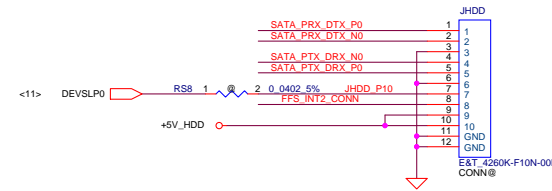
SS tableSS table



	US2	RS35	RS36	RS18	RS22	RS23	RS24	RS29
TI	SA000032X00	4.7K	4.7K	NC	NC	NC	2K	V
PARADE	SA000071U00	7.5K	NC	V	V	V	NC	NC



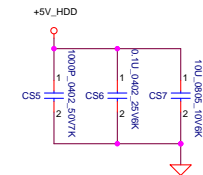
SATA HDD Connector



+5V_HDD Source

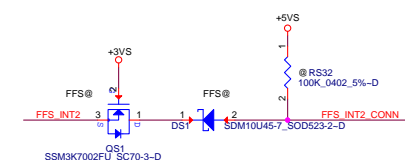
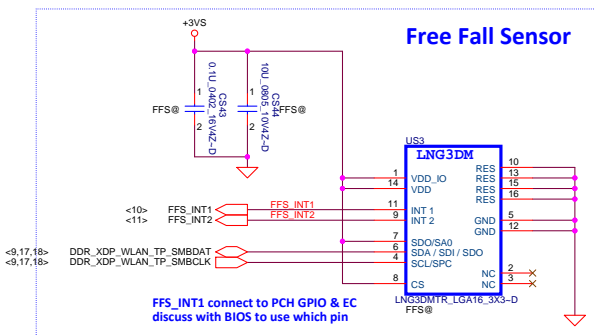


SHORT DEFAULT

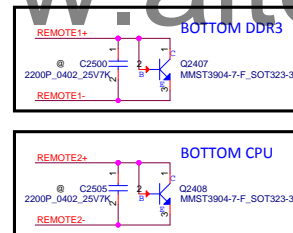
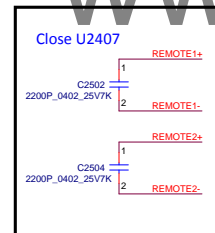
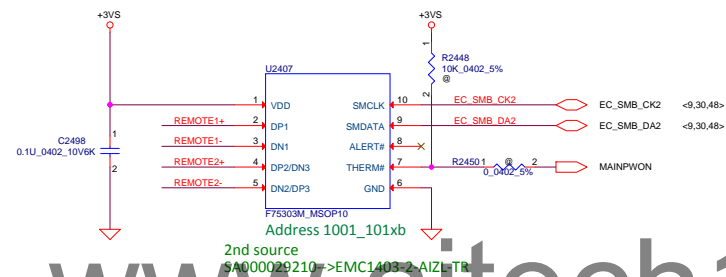


www.aitech1.ru

Free Fall Sensor

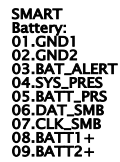
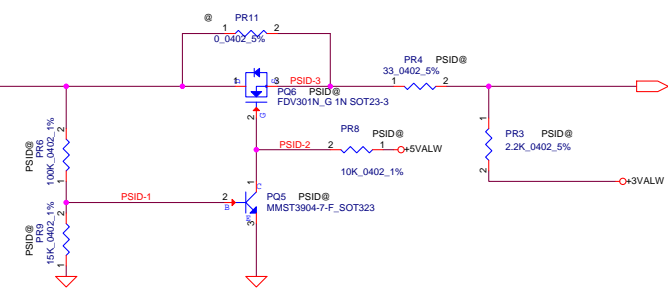


Fintek thermal sensor
placed near by TOP DDR3



REMOTE1/2 (+/-):
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title	Thermal Sensor
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-B015P
				Date	Wednesday, September 10, 2014
				Sheet	33 of 56
				Rev	0.1

[illegible]

Delay adaptor OC_H_PROCHOT#
2ms while hybrid power transition

The diagram shows a circuit for a delay adaptor. The input signal is **VCOU1_P#** (labeled <30>). This signal passes through a resistor **PR30 160K_0402_1%** to the gate of a MOSFET **PO3A L2N7000MWT1G_S028-6**. The MOSFET's source is connected to ground, and its drain is connected to the output signal **H_PROCHOT#** (labeled <30>). A capacitor **PC15 0.01uF_25V7K** is connected between the gate and the drain of the MOSFET. The MOSFET is shown in a common source configuration. The output signal **H_PROCHOT#** is then connected to a block labeled **2ms**, which represents a delay. The output of this block is the final **H_PROCHOT#** signal.

PH1 under CPU bottom side:
CPU thermal protection at 93 +/- 3 degree C

PH1 under CPU bottom side:
 CPU thermal protection at 93 +/- 3 degree C

PH1

100K_0402_1%_TSMOB104F4251RZ

<30> ECAGND

VCIN0_PH

PR24 12.1K_0402_1%

PR25 12.1K_0402_1%

+3VSW

PH1

Adapter protection:

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user

Adapter protection:

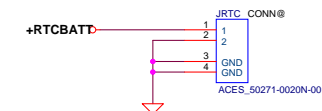
if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user



Adapter protection:

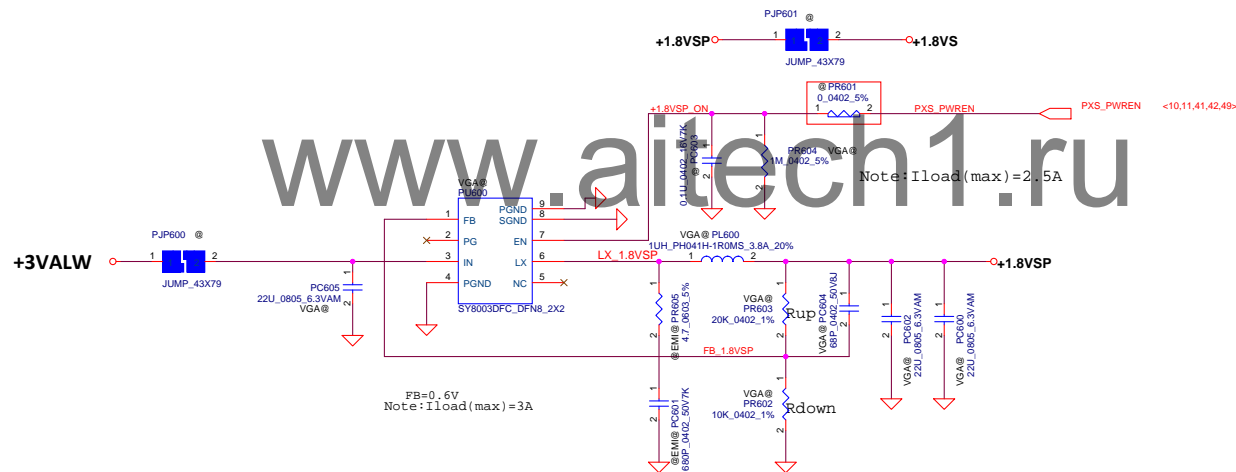
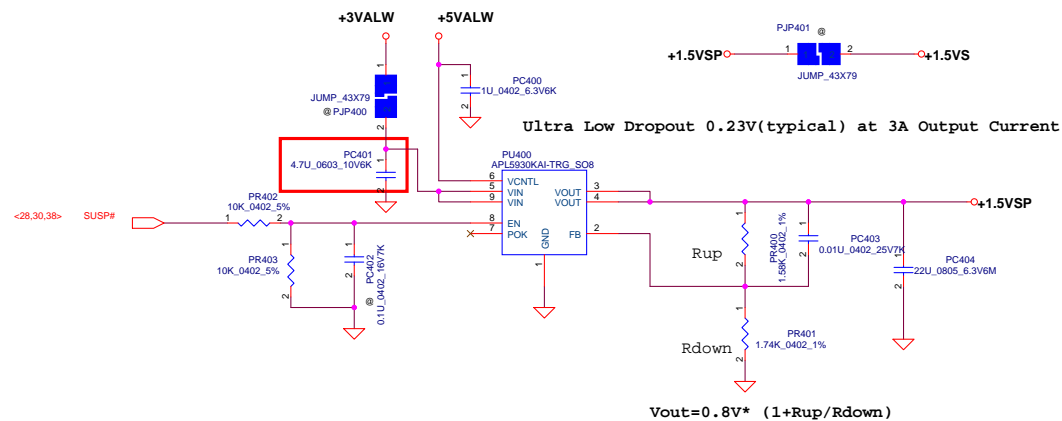
if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user

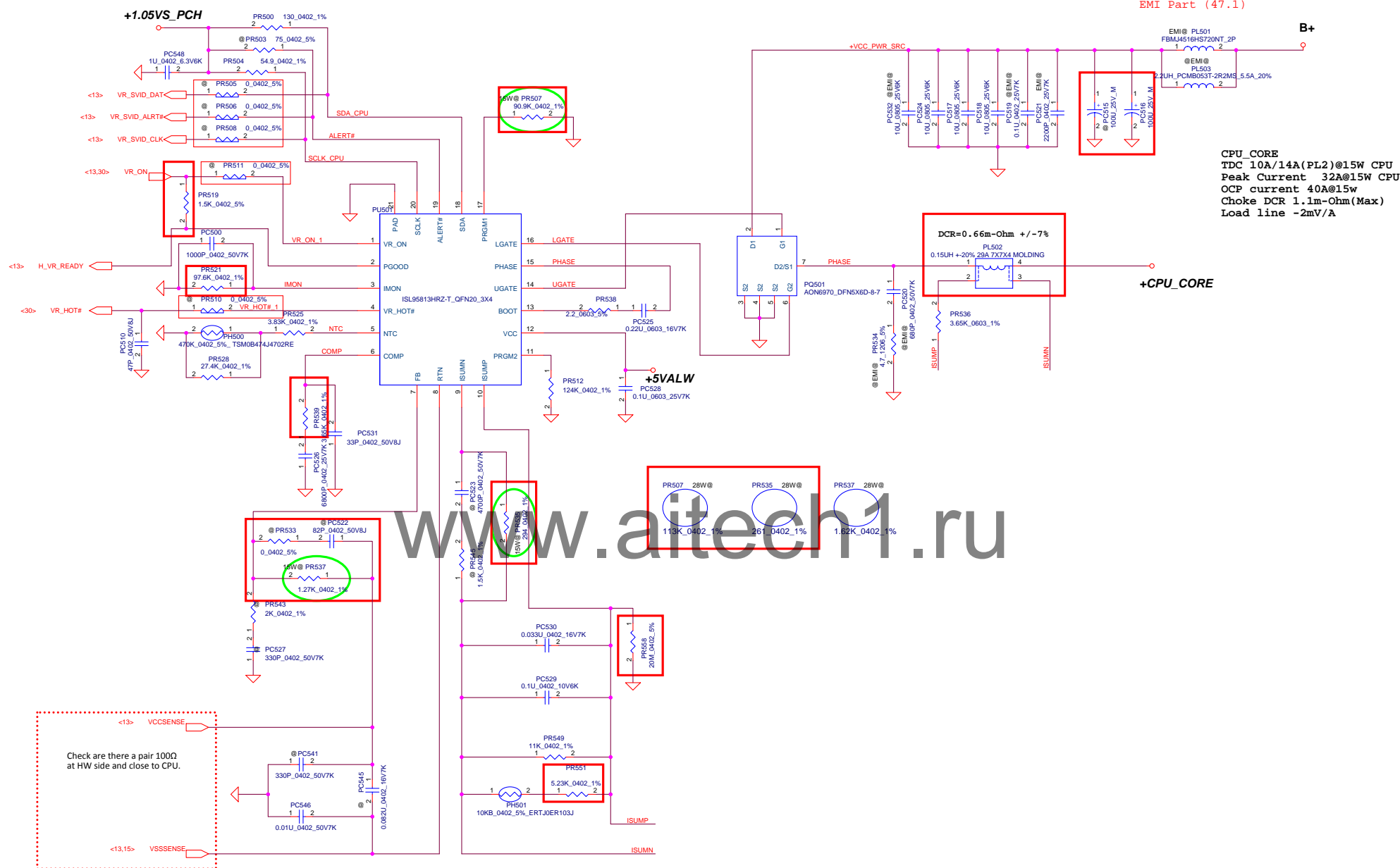
[illegible]

The diagram illustrates the 'Erp lot6 Circuit'. It features a differential signal path. On the left, a signal source labeled 'ERP_LOT6' with a value of '<30>' is connected to a resistor 'ACIN' with a value of '<10.30,35.48>'. This is followed by a resistor 'PR1' with a value of '200K_0402_1%' and a voltage source '0.1U_0402_25V6'. The signal then passes through a resistor 'PR2' with a value of '10K_0402_1%' and a component 'PG1A' labeled 'L270020W1T1G_5C28-6'. The output of this stage is connected to a resistor 'PR7' with a value of '1M_0402_1%'. The signal then passes through a resistor 'PR5' with a value of '3.3K_0201_5%' and a component 'PG1B' labeled 'L270020W1T1G_5C28-6'. The final output is connected to a resistor 'PR10' with a value of '1M_0402_1%'. The circuit is powered by 'VIN' and has a ground connection.

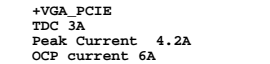
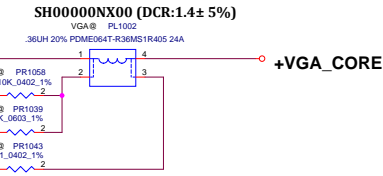
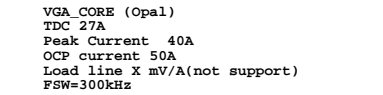
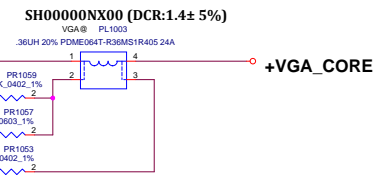
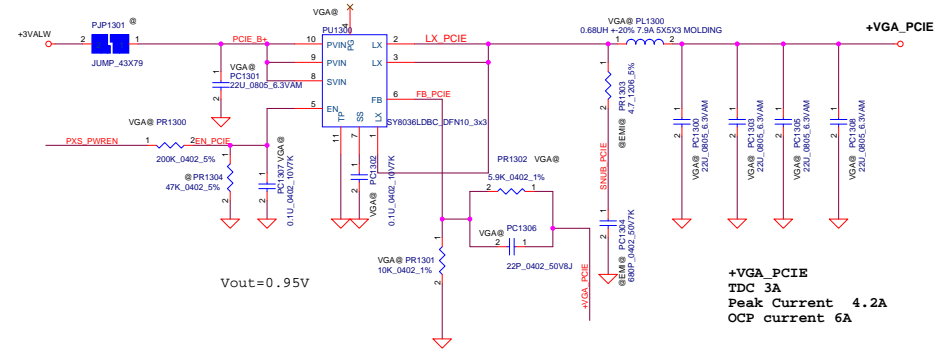
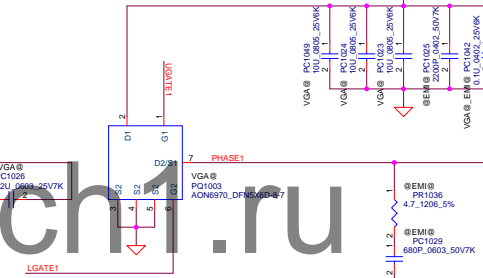
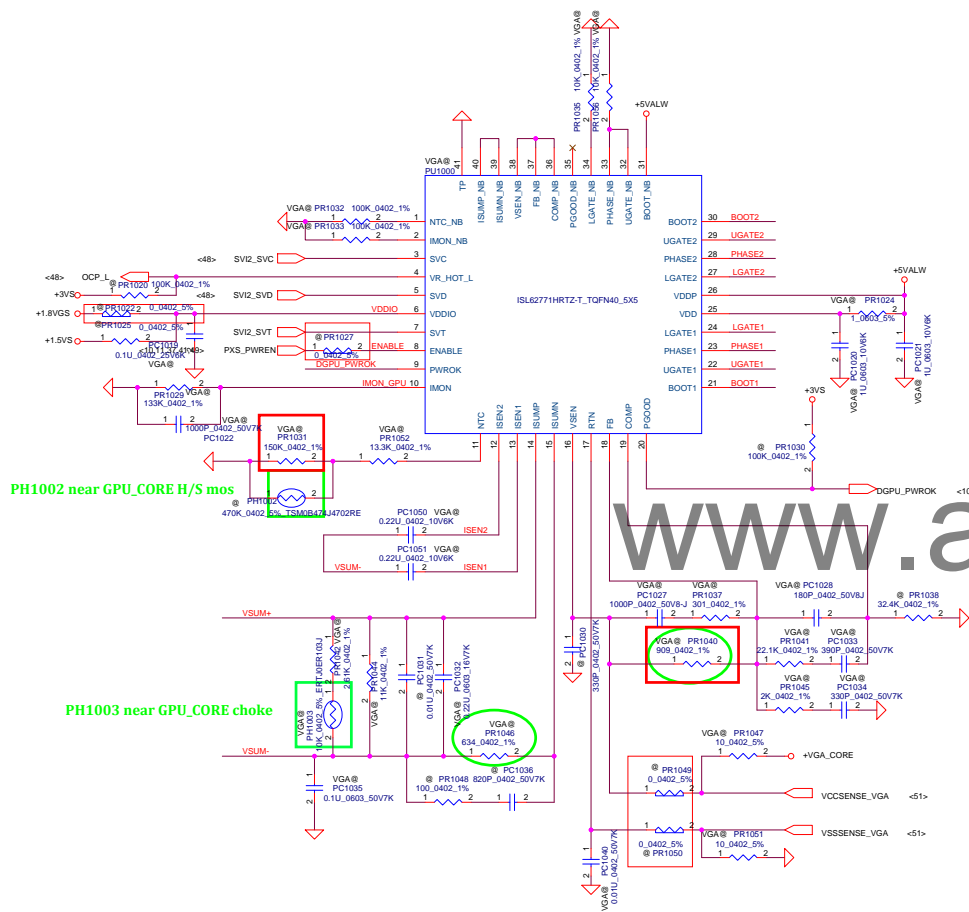


Security Classification		Compal Secret Data		<div><div></div><div>Compal Electronics, Inc.</div></div>	
Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title	<div><div></div><div>PWR DCIN/BATT CONN/OTP</div></div>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-B012P	1.0
Date:				Wednesday, September 10, 2014	Sheet 34 of 56

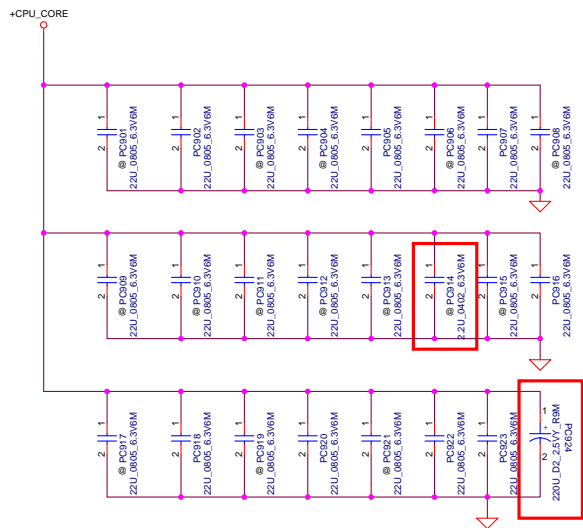




Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title	PWR +1.35VGPU	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc No	Document Number	Rev
					LA-B012P	1.0
Date:				Wednesday, September 10, 2014	Sheet	41 of 56



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				Deciphered Date				Title			
2014/01/20				2015/01/19				PWR_VGA_CORE/PCIE			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number				Rev			
				LA-B012P				1.0			
				Date				Wednesday, September 10, 2014			
				Sheet				42 of 56			



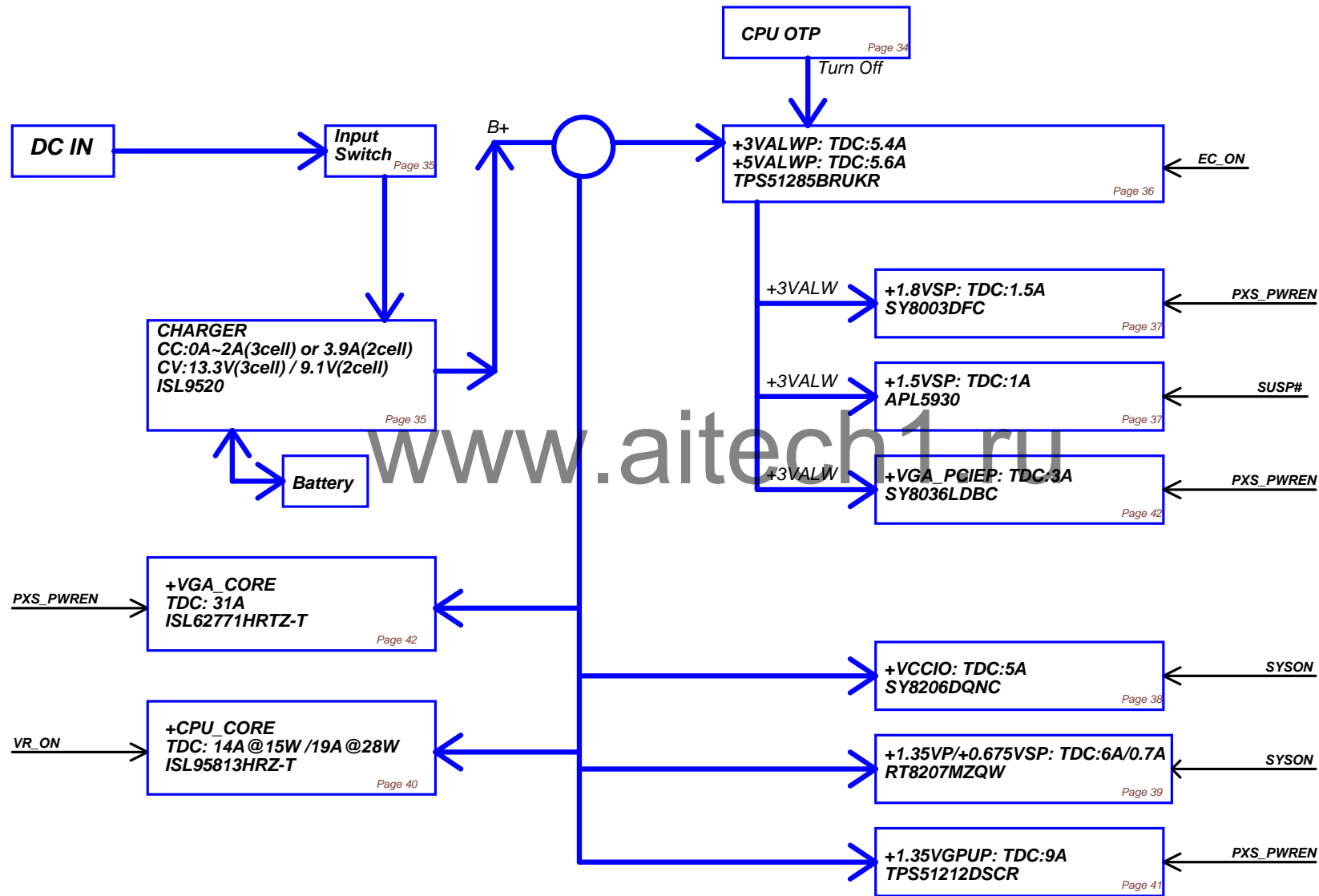
+VGA_CORE



www.aitech1.ru

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title	PWR PROCESSOR DECOUPLING
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF HONG KONG AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.				Document Number	LA-B012P
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date	Wednesday, September 10, 2014
				Sheet	43 of 56

Power block

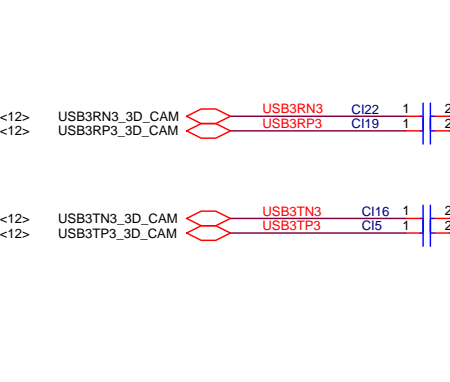
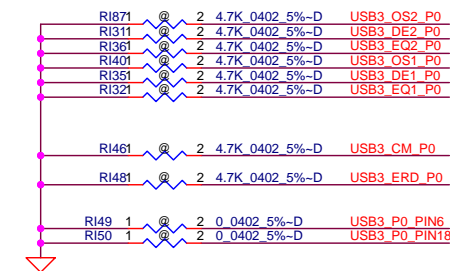
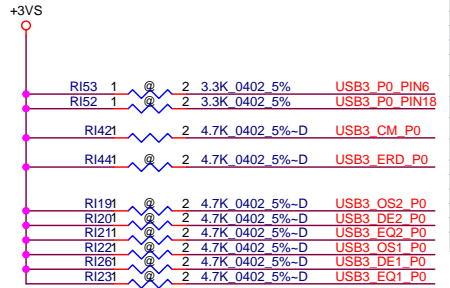


Version Change List (P. I. R. List)

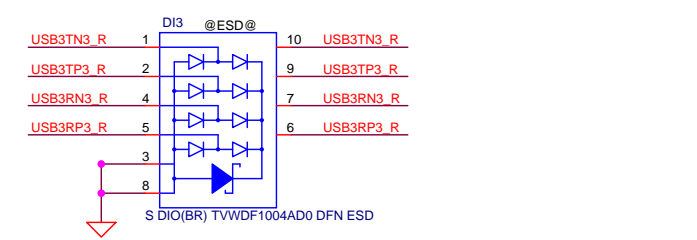
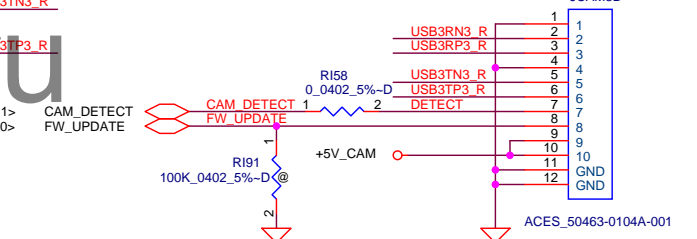
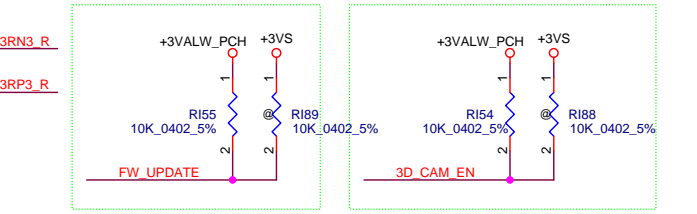
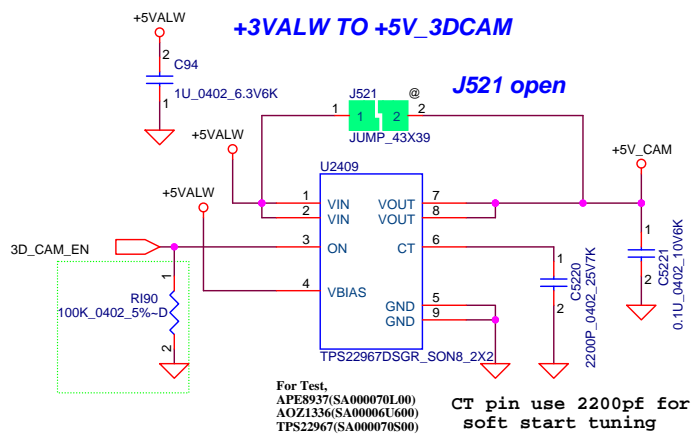
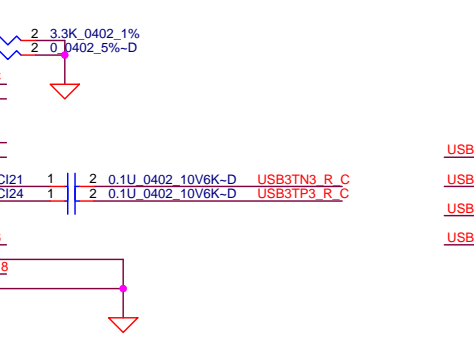
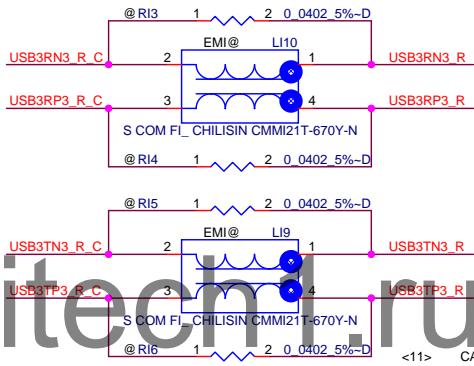
Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	DCIN/BATT CONN/OTP	13/10/24	Morris	design change	change PR16 from 100K to 10K add PR37 10K	0.2
2	45	CHARGER	13/10/24	Morris	design change	change PC711 from 1000pF to 0.01uF change PR711 from 49.9K to 51.1K change PR713 from 10K to 499K change PR724 from 100K to 499K change PC721 from 0.047u to 0.22u change PC722 from 0.1u to 1u add PC732 100u	0.2
3	46	3.3VALWP/5VALWP	13/10/24	Morris	design change for solve can't root issue	change PC104 from 0.1u to 0.22u change PC110 from 0.1u to 0.22u change PR102 from 2.2K to 10K add PR110 20K	0.2
4	50	VCORE	13/10/24	Morris	adjust CPU parameter	change PR507(15W@) from 90.9K to 169K change PR519 from 1.91K to 10K change PR521 from 95.3K to 97.6K change PR539 from 8.06K to 909 change PC515,PC516 from SF0000005100 to SF0000004M00 change PL502 from SH000000NM00 to SH000000PQ00 change PR535(15W@) from 340 to 210 change PR537 from 1.27K to 1.37K change PR535(28W@) from 432 to 261 change PR507(28W@) from 113K to 205K change PR551 from 2.61K to 5.23K add PC522 82pF add PR533 0-ohm	0.2
6	52	VGA_CORE/PCIE	13/10/24	Morris	design change from vendor change LL	change PR1040 from 1.24K to 825	0.2
7	53	PROCESSOR DECOUPLING	13/10/24	Morris	adjust CPU parameter	change PC924 from SGA20331E10 to SGA00009800 remove PC901,PC903,PC904,PC906,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC917,PC919,PC921	0.2
8	45	CHARGER	13/10/28	Morris	design change for plug out battery shut down issue	change PC723 from 0.01uF to 0.47uF change PR728 from 0 to 9.09K change PC728 from 4700pF to 2200pF change PC701 from 220pF to 1000pF	0.2
9	46	3.3VALWP/5VALWP	13/12/12	Morris	design change from EE request	add PR115 10K-ohm	0.3
10	50	VCORE	13/12/12	Morris	design change from Intel recommend	change PR519 from 10K to 1.5K	0.3
11	48	+VCCIO	13/12/13	Morris	design change from EE request	delete PR310 and add PR300 0-ohm	0.3
12	50	VCORE	14/01/20	Morris	adjust CPU parameter	change PR507(15W@) from 169K to 90.9K change PR507(28W@) from 205K to 113K	1.0
13	53	PROCESSOR DECOUPLING	14/02/13	Morris	design change from thermal request	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0
14	50	VCORE	14/03/03	Morris	design change for VGA thermal issue	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0

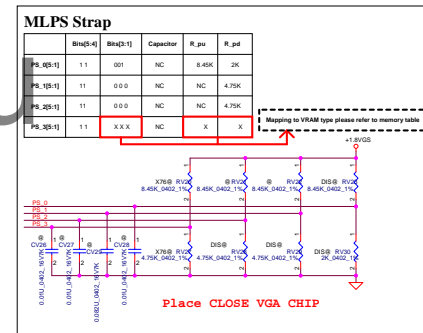
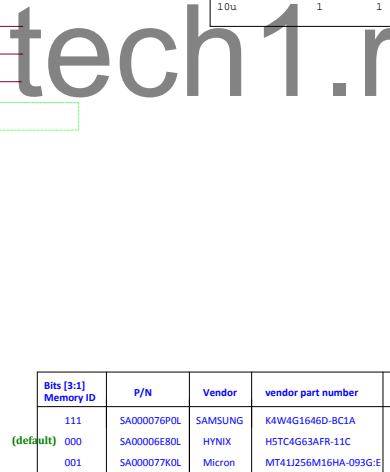
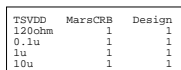
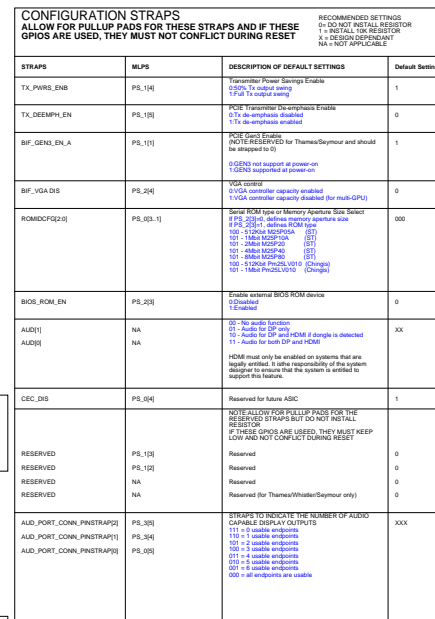
Security Classification	Compal Secret Data		Title	
Issued Date	2014/01/20	Deciphered Date	2015/01/19	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
LA-B012P				Rev 1.0
Date: Wednesday, September 10, 2014				Sheet 45 of 56



Vendor	PS8713B	TI	Spec	schematic netname	3Vs	GND
1	VDD	VCC	Same			
2	B_EQ0	EQ1	LL: 9.5dB (default) LH: 13dB HL: 4.5dB HH: 7.7 dB	USB3_EQ1_P0	R123	@ R132
3	DE0	DE1	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_DE1_P0	R126	@ R135
4	EQ1	OS1	LL: 9.5dB LH: 13dB HL: 4.5dB HH: 7.7 dB	USB3_OS1_P0	R122	@ R140
5	PD#	EN_RXD	it can be left open	USB3_ERD_P0	R144	@ R148
6	B_DE1	GND	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_P0_PIN6	R153	@ R149
7	REXT	NC	4.99K			R156 4.99K
8	B_Ina	RX1-	Same			
9	B_Inp	RX1+	Same			
10	GND	GND	Same			
11	A_OUTa	TX2-	Same			
12	A_OUTp	TX2+	Same			
13	VDD	VCC	Same			
14	TS1/NC	CM	4.7K ohm resistor for performance adjustment	USB3_CM_P0	R142	@ R146
15	A_EQ1	OS2	LL: 9.5 dB (default) LH: 13 dB	USB3_OS2_P0	R119	@ R187
16	A_DE0	DE2	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_DE2_P0	R120	@ R131
17	A_EQ0	EQ2	LL: 9.5 dB (default) LH: 13 dB	USB3_EQ2_P0	R121	@ R136
18	A_DE1	GND	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_P0_PIN18	R152	@ R150
19	A_Inp	RX2-	Same			
20	A_Ina	RX2+	Same			
21	GND	GND	Same			
22	B_OUTp	TX1+	Same			
23	B_OUTa	TX1-	Same			
24	I2C_EN	NC	this pin can be NC or connected to GND	NC		R157 @



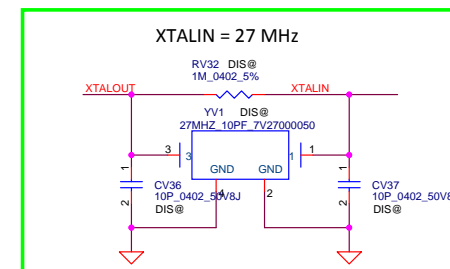
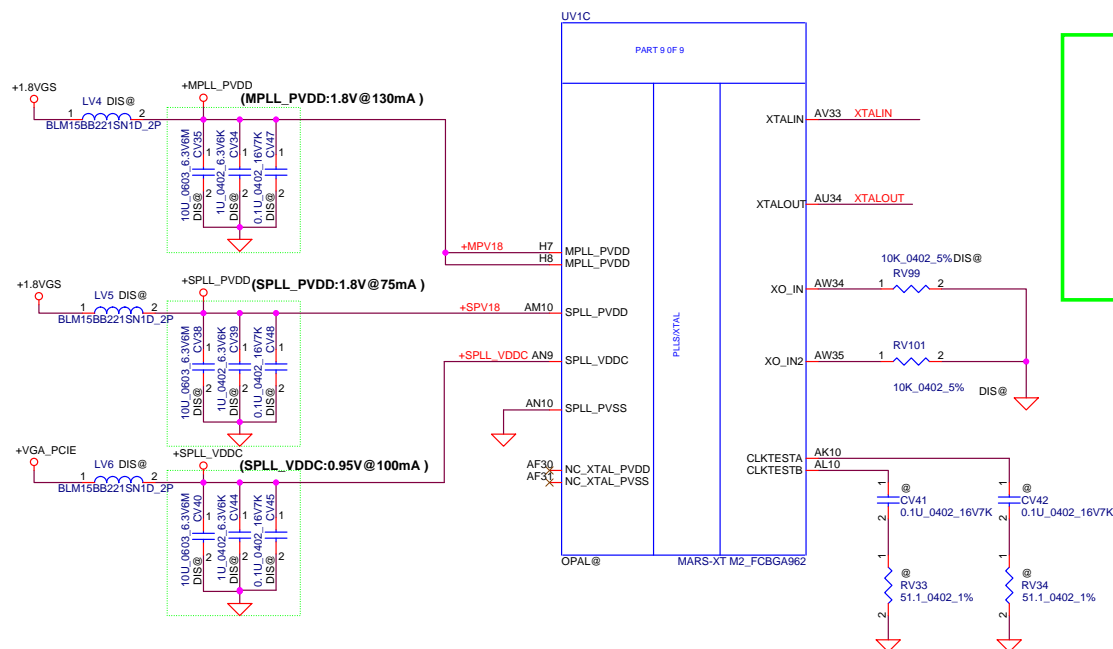
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title	3D CAMERA
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-B015P
				Date:	Wednesday, October 22, 2014
				Sheet	46 of 56



- ★Place MLPS circuit components as close to ASIC as possible
- ★Total DC resistance of trace between PS pin and C should be less than 2 ohm
- ★Total DC resistance of trace between C and ground should be less than 2 ohm
- ★Trace capacitance should be less than 100pf.
- ★Resistors should be of $\pm 1\%$ tolerance

Security Classification	Control Secret Data	Compal Electronics, Inc.
Issued Date	2014/04/01	Deciphered Date
THIS SECRET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SECRET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT TO ANY OTHER DIVISION OR AUTHORITY, OR BE DISCLOSED TO ANY OTHER PERSON OR ENTITY WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		AMD OPAL-XT M2 Main MSIC LA-B015P

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

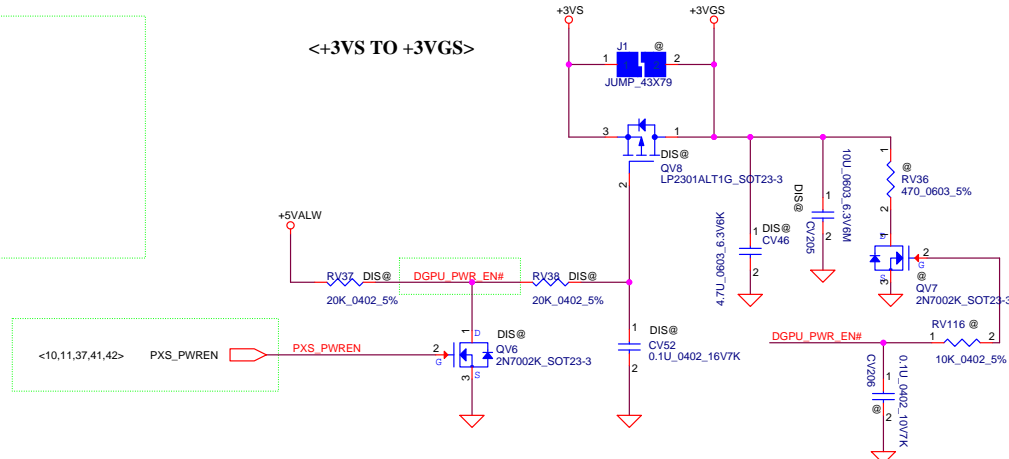


www.aitech1.ru

SHORT DEFAULT

SHORT DEFAULT

<+3VS TO +3VGS>



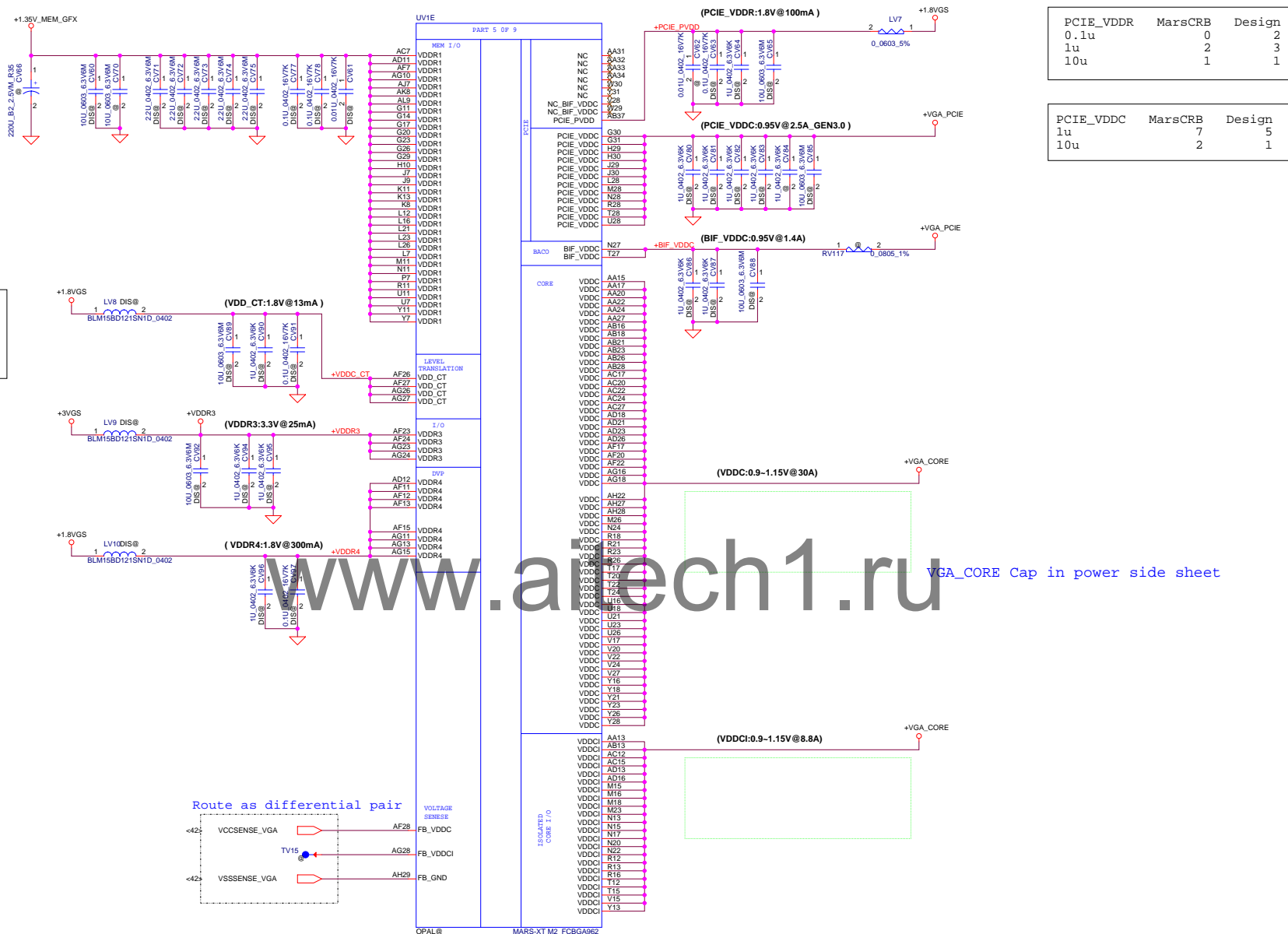
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title	AMD_OPAL-XT_M2_BACO POWER
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RADECH DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Docu- ment Number	Rev 0.
				LA-B015P	
				Date:	Wednesday, September 10, 2014 Sheet 49 of 56

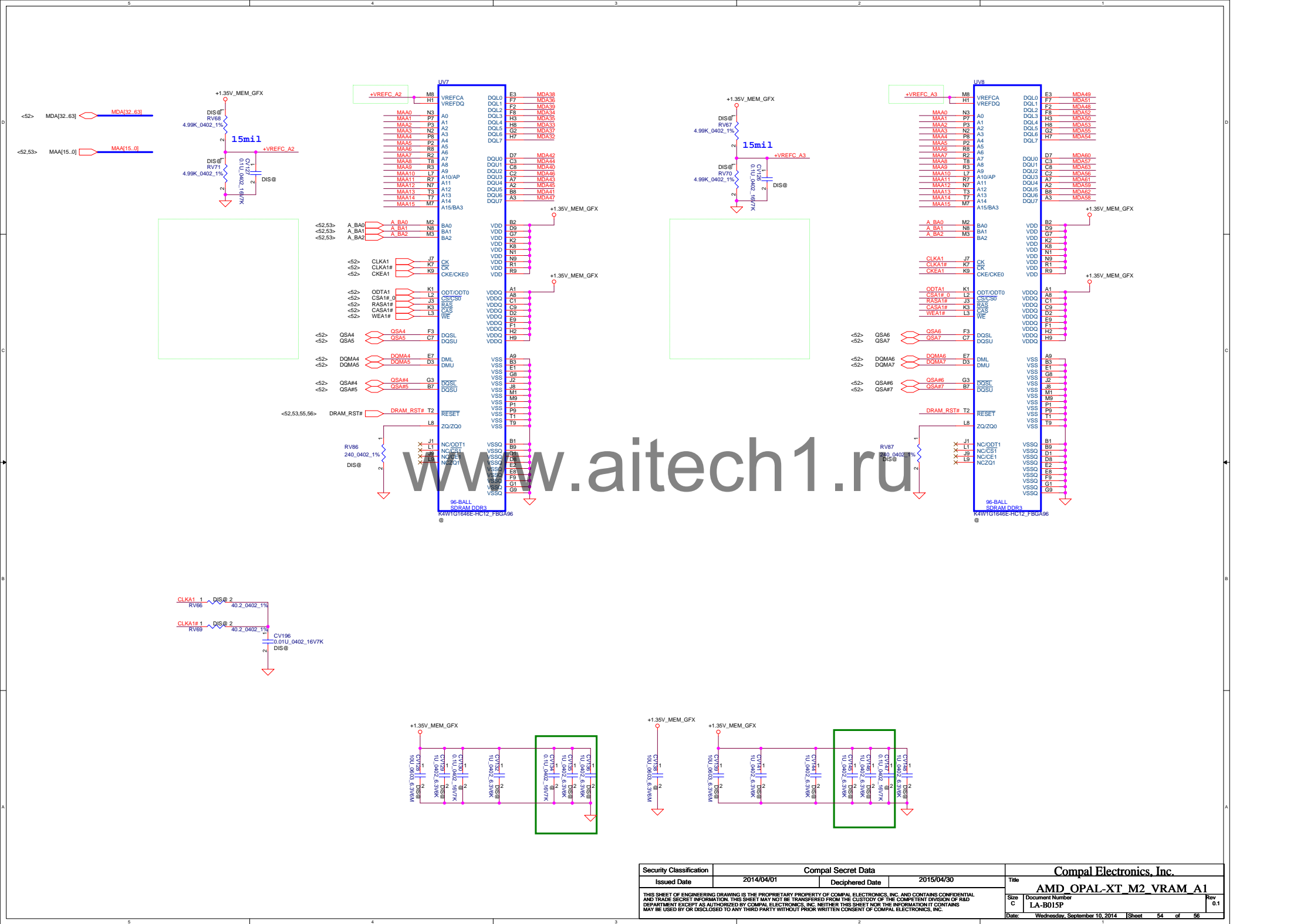
VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0





Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				AMD OPAL-XT M2_VRAM_A1	
Size	C	Document Number	LA-B015P	Rev	
Date:		Wednesday, September 10, 2014		Sheet	54 of 56

